L Number	Hits	Search Text	DB	Time stamp
1	4253	condition adj code$2	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 13:02
2	119	(condition adj code$2) near3 table$2	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 13:15
3	157	712/238.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/26 13:15

Terms used **two table branch prediction**

Found **67,988** of **139,988**

Sort results by: relevance

Display results: expanded form

Save results to a Binder

Search Tips

Open results in a new window

Try an Advanced Search

Try this search in The ACM Guide

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

Best 200 shown

Relevance scale

1 Alternative implementations of two-level adaptive branch prediction

Tse-Yu Yeh, Yale N. Patt

April 1992 **ACM SIGARCH Computer Architecture News , Proceedings of the 19th annual international symposium on Computer architecture**, Volume 20 Issue 2

Full text available: pdf(1.29 MB) Additional Information: full citation, abstract, references, citings, index terms

As the issue rate and depth of pipelining of high performance Superscalar processors increase, the importance of an excellent branch predictor becomes more vital to delivering the potential performance of a wide-issue, deep pipelined microarchitecture. We propose a new dynamic branch predictor (Two-Level Adaptive Branch Prediction) that achieves substantially higher accuracy than any other scheme reported in the literature. The mechanism uses two levels of branch history information to make ...

2 Alternative implementations of two-level adaptive branch prediction

Tse-Yu Yeh, Yale N. Patt

August 1998 **25 years of the international symposia on Computer architecture (selected papers)**

Full text available: pdf(1.39 MB) Additional Information: full citation, references, index terms

3 Two-level adaptive training branch prediction

Tse-Yu Yeh, Yale N. Patt

September 1991 **Proceedings of the 24th annual international symposium on Microarchitecture**

Full text available: pdf(1.13 MB) Additional Information: full citation, references, citings, index terms

4 The role of adaptivity in two-level adaptive branch prediction

Stuart Sechrest, Chih-Chieh Lee, Trevor Mudge

December 1995 **Proceedings of the 28th annual international symposium on Microarchitecture**

Full text available: pdf(656.63 KB) Additional Information: full citation, references, citings, index terms

5 A comparison of dynamic branch predictors that use two levels of branch history

Tse-Yu Yeh, Yale N. Patt

May 1993 **ACM SIGARCH Computer Architecture News , Proceedings of the 20th annual international symposium on Computer architecture**, Volume 21 Issue 2

Full text available: pdf(987.31 KB) Additional Information: full citation, abstract, references, citings, index terms

Recent attention to speculative execution as a mechanism for increasing performance of single instruction streams has demanded substantially better branch prediction than what has been previously available. We [1,2] and Pan, So, and Rahmen [4] have both proposed variations of the same aggressive dynamic branch predictor for handling those needs. We call the basic model Two-Level Adaptive Branch Prediction; Pan, So, and Rahmeh call it Correlation Branch Prediction. In this paper, we adopt th ...

6 Regular contributions: An alternative to branch prediction: pre-computed branches

Lucian N. Vintan, Marius Sbera, Ioan Z. Mihu, Adrian Florea

June 2003 **ACM SIGARCH Computer Architecture News**, Volume 31 Issue 3

Full text available: pdf(985.31 KB) Additional Information: full citation, abstract, references

Through this paper we developed an alternative approach to the present -- day two level dynamic branch prediction structures. Instead of predicting branches based on history information, we propose to pre - calculate the branch outcome. A pre - calculated branch prediction (PCB) determines the outcome of a branch as soon as all of the branch's operands are known. The instruction that produced the last branch's operand will trigger a supplementary branch condition estimation and, after this opera ...

Keywords: complexity evaluations, dynamic branch prediction, execution driven simulation, multiple instruction issue, performance, pipelining, speculative execution

7 Neural methods for dynamic branch prediction

Daniel A. Jiménez, Calvin Lin

November 2002 **ACM Transactions on Computer Systems (TOCS)**, Volume 20 Issue 4

Full text available: pdf(540.67 KB) Additional Information: full citation, abstract, references, index terms

This article presents a new and highly accurate method for branch prediction. The key idea is to use one of the simplest possible neural methods, the perceptron, as an alternative to the commonly used two-bit counters. The source of our predictor's accuracy is its ability to use long history lengths, because the hardware resources for our method scale linearly, rather than exponentially, with the history length. We describe two versions of perceptron predictors, and we evaluate these predictors ...

Keywords: Branch prediction, neural networks

8 An analysis of dynamic branch prediction schemes on system workloads

Nicolas Gloy, Cliff Young, J. Bradley Chen, Michael D. Smith

May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd annual international symposium on Computer architecture**, Volume 24 Issue 2

Full text available: pdf(1.21 MB) Additional Information: full citation, abstract, references, citings, index terms

Recent studies of dynamic branch prediction schemes rely almost exclusively on user-only simulations to evaluate performance. We find that an evaluation of these schemes with user and kernel references often leads to different conclusions. By analyzing our own Atom-generated system traces and the system traces from the Instruction Benchmark Suite, we quantify the effects of kernel and user interactions on branch prediction accuracy. We find that user-only traces yield accurate prediction results ...

Keywords: 2-level adaptive prediction, branch prediction, correlation, system traces

9 Branch history table indexing to prevent pipeline bubbles in wide-issue superscalar processors

Tse-Yu Yeh, Yale N. Patt

December 1993 **Proceedings of the 26th annual international symposium on Microarchitecture**

Full text available: pdf(1.44 MB) Additional Information: full citation, references, citings

10 Increasing the instruction fetch rate via multiple branch prediction and a branch address cache

Tse-Yu Yeh, Deborah T. Marr, Yale N. Patt

August 1993 **Proceedings of the 7th international conference on Supercomputing**

Full text available: pdf(1.13 MB) Additional Information: full citation, references, citings, index terms, review

11 Implementation and analysis of path history in dynamic branch prediction schemes

S. Reches, S. Weiss

July 1997 **Proceedings of the 11th international conference on Supercomputing**

Full text available: pdf(954.47 KB) Additional Information: full citation, references, index terms

12 The cascaded predictor: economical and adaptive branch target prediction

Karel Driesen, Urs Hölzle

November 1998 **Proceedings of the 31st annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(1.87 MB) Additional Information: full citation, references, citings, index terms

13 Circuit considerations for low power: Branch prediction on demand: an energy-efficient solution

Daniel Chaver, Luis Piñuel, Manuel Prieto, Francisco Tirado, Michael C. Huang

August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**

Full text available: pdf(151.23 KB) Additional Information: full citation, abstract, references, index terms

High-end processors typically incorporate complex branch predictors consisting of many large structures that together consume a notable fraction of total chip power (more than 10% in some cases). Depending on the applications, some of these resources may remain underused for long periods of time. We propose a methodology to reduce the energy consumption of the branch predictor by characterizing prediction demand using profiling and dynamically adjusting predictor resources accordingly. Specifica ...

Keywords: adaptive, branch prediction, profiling

14 The effects of predicated execution on branch prediction

Gary Scott Tyson

November 1994 **Proceedings of the 27th annual international symposium on Microarchitecture**

Full text available: pdf(1.20 MB) Additional Information: full citation, abstract, references, citings, index terms

High performance architectures have always had to deal with the performance limiting impact of branch operations. Microprocessor designs are going to have to deal with this problem as well, as they move towards deeper pipelines and support for multiple instruction issue. Branch prediction schemes are often used to alleviate the negative impact of branch operations by allowing the speculative execution of instructions after an unresolved branch. Another technique is to eliminate branch instr ...

Keywords: ATOM, Alpha, HP-RISC, Pentium, PowerPC, branch prediction, high-performance, predication

15 Fast and accurate instruction fetch and branch prediction

B. Calder, D. Grunwald

April 1994 **ACM SIGARCH Computer Architecture News , Proceedings of the 21ST annual international symposium on Computer architecture**, Volume 22 Issue 2

Full text available: pdf(1.07 MB) Additional Information: full citation, abstract, references, citings, index terms

Accurate branch prediction is critical to performance; mispredicted branches mean that ten's of cycles may be wasted in superscalar architectures. Architectures combining very effective branch prediction mechanisms coupled with modified branch target buffers (BTB's) have been proposed for wide-issue processors. These mechanisms require considerable processor resources. Concurrently, the larger address space of 64-bit architectures introduce new obstacles and opportunities. A larger address space ...

16 Speculative execution and branch prediction on parallel machines

Kevin B. Theobald, Guang R. Gao, Laurie J. Hendren

August 1993 **Proceedings of the 7th international conference on Supercomputing**

Full text available: pdf(1.28 MB) Additional Information: full citation, abstract, references, citings, index terms

Several recent studies on the limits of parallelism have reported that speculative execution can substantially increase the amount of exploitable parallelism in programs, especially non-numerical programs. This is true even for parallel machines models which allow multiple flows of control. However, most architectural techniques for speculation and branch prediction are geared toward conventional computers with a single flow of control, and little has been done in studying ...

17 Accurate indirect branch prediction

Karel Driesen, Urs Hölzle

April 1998 **ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual international symposium on Computer architecture**, Volume 26 Issue 3

Full text available: pdf(1.49 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Indirect branch prediction is likely to become increasingly important in the future because indirect branches occur more frequently in object-oriented programs. With misprediction rates of around 25% on current processors, indirect branches can incur a significant fraction of branch misprediction overhead even though they remain less frequent than the more predictable conditional branches. We investigate a wide range of two-level predictors dedicated exclusively to indirect branches. Starting wi ...

18 Assigning confidence to conditional branch predictions

Erik Jacobsen, Eric Rotenberg, J. E. Smith

December 1996 **Proceedings of the 29th annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(1.28 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Many high performance processors predict conditional branches and consume processor resources based on the prediction. In some situations, resource allocation can be better optimized if a confidence level is assigned to a branch prediction; i.e. if the quantity of resources allocated is a function of the confidence level. To support such optimizations, we consider hardware mechanisms that partition conditional branch predictions into two sets: those which are accurate a relatively high percentag ...

Keywords: branch correctness, conditional branch predictions, dynamic branches,

processor resources, resource allocation, static branches

19 Compiler synthesized dynamic branch prediction

Scott Mahlke, Balas Natarajan

December 1996 **Proceedings of the 29th annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(1.50 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Branch prediction is the predominant approach for minimizing the pipeline breaks caused by branch instructions. Traditionally, branch prediction is accomplished in one of two ways, static prediction at compile-time via compiler analysis or dynamic prediction at run-time via special hardware structures. In this paper, we propose a novel technique that aims to combine the strengths of the two approaches -- the lower cost of compile-time analysis with the effectiveness of dynamic prediction. Specif ...

Keywords: branch instruction, compiler analysis, dynamic branch prediction, pipelined processor, profile information

20 Evidence-based static branch prediction using machine learning

Brad Calder, Dirk Grunwald, Michael Jones, Donald Lindsay, James Martin, Michael Mozer, Benjamin Zorn

January 1997 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 19 Issue 1

Full text available: pdf(515.50 KB) Additional Information: full citation, abstract, references, citings, index terms

Correctly predicting the direction that branches will take is increasingly important in today's wide-issue computer architectures. The name program-based branch prediction is given to static branch prediction techniques that base their prediction on a program's structure. In this article, we investigate a new approach to program-based branch prediction that uses a body of existing programs to predict the branch behavior in a new program. We call this approach to program-ba ...

Keywords: branch prediction, decision trees, machine learning, neural networks, performance evaluation, program optimization